

### **ABSTRACT OF DISCLOSURE**

An apparatus for adjusting a sampling phase in analog to digital conversion, and an adjustment method thereof is disclosed. Provided are an apparatus for adjusting a sampling phase of a digital display including a phase locked loop (PLL) circuit unit for converting a frequency of a sampling clock signal and outputting the converted frequency, the sampling clock signal for converting an analog video signal into digital format, an analog to digital converter (ADC) for converting the incoming analog video signal into digital format using the sampling clock signal input from the PLL circuit unit, a detection unit for detecting a maximum phase shift of the video signal converted at the ADC, and a control unit for controlling the PLL circuit unit so that the sampling phase can be adjusted in accordance with the maximum phase shift detected by the detection unit, and an adjustment method of the apparatus.